

## IN THE CLAIMS

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1. (previously presented) A process of forming a container cell, comprising:

forming a trench in a semiconductor substrate, said semiconductor substrate having an upper surface;

forming an isolation film within said trench;

forming a gate oxide on the upper surface of said semiconductor substrate such that the gate oxide extends below the upper surface of said semiconductor substrate;

forming a first gate stack upon said semiconductor substrate and having an edge aligned with and adjacent to an edge of said trench;

forming a second gate stack upon said isolation film within said trench; and

etching a container cell into said isolation film within said trench, said container cell being situated substantially between said first and second gate stacks and having an edge defined by said semiconductor substrate and said isolation film, said edge of said container cell substantially extending to and terminating at each of said first and second gate stacks.

2. (previously presented) A process of forming a container cell as defined in Claim 1, wherein etching a container cell etches said semiconductor substrate such that a portion of said container cell extends beneath said first gate stack.

3. (original) A process of forming a container cell as defined in Claim 1, wherein forming a trench comprises spinning on a photoresist, masking, exposing and patterning said

photoresist to create a photoresist mask, and anisotropically etching through said photoresist mask.

4. (original) A process of forming a container cell as defined Claim 1, wherein said isolation film is a TEOS film.

5. (original) A process of forming a container cell as defined Claim 1, wherein said isolation film is a PSG film.

6. (original) A process of forming a container cell as defined Claim 1, wherein said isolation film is a BPSG film.

7. (original) A process of forming a container cell as defined in Claim 1, wherein forming a first gate stack and forming a second gate stack include forming a silicon nitride spacer, respectively, upon said first and said second gate stacks.

8. (previously presented) A process of forming a container cell as defined in Claim 1, wherein etching a container cell comprises an RIE process.

9. (original) A process of forming a container cell as defined in Claim 1, further comprising:

forming a first polycrystalline silicon layer within said container cell;

depositing a cell dielectric upon said first polycrystalline silicon layer; and

depositing a second polycrystalline silicon layer continuously upon said first gate stack, upon said cell dielectric, and upon said second gate stack.

10. (original) A process of forming a container cell as defined in Claim 9, wherein said first polycrystalline silicon layer is formed by an in-situ doping CVD process.

11. (original) A process of forming a container cell as defined in Claim 9, wherein said second polycrystalline silicon layer is formed by an in-situ doping CVD process.

12. (original) A process of forming a container cell as defined in Claim 1, wherein said isolation film and said semiconductor substrate have an interface below said container cell.

13. (original) A process of forming a container cell as defined in Claim 1, wherein said isolation film and said semiconductor substrate have an interface below said container cell, such that said interface is coplanar with said edge defined by said semiconductor substrate and said isolation film.

14. (original) A process of forming a container cell as defined in Claim 1, wherein said isolation film and said semiconductor substrate have an interface below said container cell, such that said interface is not coplanar with said edge defined by said semiconductor substrate and said isolation film.

15. (previously presented) A process of forming a container cell, comprising:

forming a trench in a semiconductor substrate, said semiconductor substrate having an upper surface;

forming a conformal isolation film within said trench;

growing a gate oxide on the upper surface of said semiconductor substrate such that the gate oxide extends below the upper surface of said semiconductor substrate;

forming a first gate stack upon said semiconductor substrate and having an edge aligned with and adjacent to an edge of said trench;

forming a second gate stack upon said isolation film within said trench; and

etching a container cell into said isolation film within said trench, said container cell being situated substantially between said first and second gate stacks and having an edge defined by said semiconductor substrate and said isolation film, said edge of said container cell substantially extending to and terminating at each of said first and second gate stacks, wherein said semiconductor substrate and said isolation film have an interface that extends below said edge into said semiconductor substrate.

16. (previously presented) A process of forming a container cell as defined in Claim 15, wherein forming an isolation film is performed by forming an oxide film by the decomposition of TEOS.

17. (original) A process of forming a container cell as defined in Claim 15, wherein said container cell is electrically isolated between said isolation film and said semiconductor substrate.

18. (previously presented) A process of forming a container cell as defined in Claim 15, wherein etching a container cell comprises an RIE process.

19. (previously presented) A process of forming a container cell, comprising:

forming a trench in a semiconductor substrate by spinning on a photoresist, masking, exposing and patterning said photoresist to create a photoresist mask, and anisotropically etching through said photoresist mask, said semiconductor substrate having an upper surface;

forming a conformal isolation film within said trench by forming an oxide film by deposition;

growing a gate oxide on the upper surface of said semiconductor substrate such that the gate oxide extends below the upper surface of said semiconductor substrate;

forming a first gate stack upon said semiconductor substrate and having an edge aligned with and adjacent to an edge of said trench;

forming a second gate stack upon said isolation film within said trench; and

etching a container cell into said isolation film within said trench, said container cell being situated substantially between said first and second gate stacks and having an edge defined by said semiconductor substrate and said isolation film, said edge of said container cell substantially extending to and terminating at each of said first and second gate stacks, wherein said semiconductor substrate and said isolation film form an interface that extends below said container cell into said semiconductor substrate.

20. (previously presented) A process of forming a container cell as defined in Claim 19, wherein said edge and said interface are coplanar.

21. (previously presented) A process of forming a container cell as defined in Claim 19, wherein said edge and said interface are not coplanar.

22. (original) A process of forming a container cell as defined in Claim 19, further comprising:

forming a first polycrystalline silicon layer within said container cell;  
depositing a cell dielectric upon said first polycrystalline silicon layer; and  
depositing a second polycrystalline silicon layer continuously upon said first gate stack, upon said cell dielectric, and upon said second gate stack.

23. (previously presented) A process of forming a capacitor, comprising:

forming a trench in a semiconductor substrate, said semiconductor substrate having an upper surface;

forming an isolation film within said trench;

forming a gate oxide on the upper surface of said semiconductor substrate such that the gate oxide extends below the upper surface of said semiconductor substrate;

forming a first gate stack upon said semiconductor substrate, said first gate stack having an edge aligned with and adjacent to an edge of said trench;

forming a second gate stack upon said isolation film within said trench;

etching a container cell into said isolation film within said trench, said container cell being situated substantially between said first and second gate stacks and having an edge defined by said semiconductor substrate and said isolation film, said edge of said container cell substantially extending to and terminating at each of said first and second gate stacks;

forming a storage node within said container cell;

forming a cell dielectric upon said storage node; and

forming a cell plate upon said first gate stack, upon said cell dielectric, and upon said second gate stack.

24. (cancelled)

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